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Review article

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Transistor engineering based on 2D materials in the post-silicon era

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Abstract

The miniaturization of metal–oxide–semiconductor field-effect transistors (MOSFETs) has been the driving force behind the development of integrated circuits over the past 60 years; however, owing to short channel effect, reducing the gate length of MOSFETs to sub-10 nm represents a fundamental challenge. Two-dimensional materials (2DMs) with atomic scale thicknesses and non-dangling bonds interface enable sub-10 nm scale length, making them suitable candidates for advanced tech nodes beyond sub-3 nm. Although the performance metrics of a single 2DMs transistor have equalled or surpassed those of silicon, leaving no doubt about the potential of 2DMs at the laboratory level, the way of moving 2DMs from 'lab to fab' remains unclear. In this Review, we analyse the similarities and differences between 2DMs MOSFETs and silicon MOSFETs in the integrated circuits engineering process; we present potential solutions for channel, contact and dielectric engineering using 2DM to address the scaling challenges faced by a silicon-based device at the advanced tech node. Finally, we summarize the challenges in translating the performance of individual 2DMs devices into large-scale integrated circuits, including large-scale and stable transfer technology, high-quality material synthesis with controllable layers. Once these technical issues are properly solved, 2DMs can take full advantage of their properties at a farther scaling.

Sections

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Introduction

Metal–oxide–semiconductor field-effect transistors (MOSFETs) and complementary metal–oxide–semiconductor (CMOS) circuits are the cornerstone of integrated circuits and have been the driving force behind modern technological advancement[1,2]. For large-scale integrated circuit applications, the continuous reduction in physical size of MOSFETs enables higher overall efficiency[3–5] through the gains in performance, power, area, cost and so on.

Device scaling informed by Moore's law has been the primary means by which the semiconductor industry has achieved unprecedented advances in productivity and performance. Traditionally, these advances have been driven by the development of new lithographic tools, masks, photoresist materials and key-size etching processes[6,7]. In the early days of integrated circuit development, the efforts were focused on reducing the physical gate oxide thickness and engineering the source, drain and channel doping profile. However, owing to short channel effect (SCE), the planar scaling of the transistor faces stagnation[8]. Novel device architectures such as silicon-on-insulator[9–11], fin field-effect transistors (FETs)[12–14] and gate-all-around FETs[15–17] have been introduced to improve the gate control capability and to suppress SCE. However, owing to the large parasitic capacitance induced by the 3D structure, the structural instability with high-aspect-ratio channel stack and the small spacing that makes high-*k* metal gate formation and source/drain epitaxy very difficult, the physical gate length is hard to get smaller than ~10 nm (ref. 18), below which the devices face fundamental limitations, that is, critical parts of the device cannot scale down below a few atoms in length and thickness[19]. At the atomic scale, strong charge scattering and quantum effects arise in a silicon transistor, making the material itself the main limitation[6]. Therefore, continued device scaling requires the introduction of new materials[20].

Two-dimensional semiconductors are layered materials consisting of single or few layers of atoms, the atoms in the layers are held together by saturated covalent bonds and typically the thickness of the monolayer 2D materials (2DMs) is less than 1 nm (refs. 21,22). Owing to the inert and dangling-bond-free surface, the interface between different 2DMs is nearly defect-free. As a result, the charge carrier mobility in ultra-thin 2D semiconductors can be potentially very high owing to minimized lattice defects and charge scattering[23,24]. In addition, the phonon scattering mechanism of 2DMs also contributes to high intrinsic mobility[25]. Typical 2DMs, such as MoS_2, WS_2, WSe_2, $MoTe_2$, InSe and so on, have shown excellent electronic performance in ultra-short gate length or ultra-thin channel FETs[26–30]. Because the SCE is largely suppressed, 2DMs provide an opportunity for the continued physical scaling of transistors, making them a potential material choice for future advanced nodes[31]. Exploring 2DMs in prototype devices has shown much promise[32–34] but these laboratory-scale technologies are yet to be tested in real industrial settings. Drawing on experience from silicon MOSFET technologies can provide valuable insights into ensuring 2DMs compatibility with the existing production lines towards large-scale integration (Fig. 1).

In this Review, we compare silicon-based MOSFET and 2DMs-based MOSFET technologies to reveal the key scientific issues and the corresponding performance optimization routes to achieve further scaling. On the basis of the structure of a typical transistor, we analyse the device engineering from three perspectives: channel engineering, contact engineering and dielectric engineering. In each section, we fully discuss the advantages of 2DM under ultimate scaling and promising solutions to different engineering problems. In addition, we discuss the challenges of bringing 2DMs transistor devices to large-scale integration, including the manufacturing process of MOSFET, large-scale transfer and high-quality material synthesis, in delivering the future industrialization of the advanced tech node.

Channel engineering for ultimate scaling

Dennard's law, which has informed the scaling of integrated circuits for many decades[19,35], states that the size of transistors shrinks by 30% (0.7 times) in each generation of technology, reducing their area by 50%. In terms of performance, for each technological iteration, 30% lower latency and 40% increase in operating frequency would be expected[36]. Moreover, to keep the electric field constant, the voltage, energy and power have to be reduced by 30%, 65% and 50%, respectively[37]. To keep Moore's law going and to increase the number of devices per chip, the scaling of transistors has to follow the suit. According to the scale length theory, to improve performance and reduce power consumption, the key device parameters, such as gate length, channel thickness and oxide thickness, need to be scaled down with a uniform ratio. When applied to the planar transistor, this guiding principle has provided a long-term economically viable and resource-efficient solution for the semiconductor technology development. However, the SCE issue prevents further scaling of planar transistors.

In a traditional CMOS with a planar gate structure, the characteristic gate length for the onset of SCEs can be calculated as[38]:

$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{ox}} \cdot t_{ch} t_{ox}}$$

in which t_{ch} is the thickness of a semiconducting channel, t_{ox} is the thickness of the gate dielectric and ε_{ch} and ε_{ox} are the dielectric constants of the channel and gate dielectric, respectively. To suppress SCE and to enhance the electrostatic gate control, fin FET and gate-all-around structures have been successively adopted. In the multigates transistor structure, the characteristic gate length can be smaller, which can be expressed as[39]:

$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{2\varepsilon_{ox}} \cdot t_{ch} t_{ox}}$$

This means that for the same effective gate length, the multigates structure would have better subthreshold behaviour than a planar structure. The minimum channel length could be reduced by 30% and could obtain better subthreshold characteristics. However, according to the technical path diagram of the International Roadmap for Devices and Systems (IRDS), the channel thickness in the sub-5 nm node is limited to a minimum of 6 nm (ref. 31). It can be seen that even if the structural design is adopted to reduce the SCE, the physical thickness of silicon limits the effective mobility, thus making it impossible for the device to scale further (Fig. 2a). Owing to the flat surface of the 2DM, lattice scattering is suppressed at the atomic thickness, thus maintaining high mobility at a sub-1 nm thickness. This quality represents a prominent advantage for the ultimate transistor scaling. Additionally, 2DMs are particularly suited for future potential transistor architectures such as multibridge-channel FETs and complementary FETs[40–43]. A typical monolayer 2D semiconductor, such as MoS_2, has a low dielectric constant (~4) and a sizable bandgap (~1.8 eV), which can enhance electrostatic controllability and ensure low leakage[44]. Following the aforementioned equations, the characteristic gate length for 2DM transistors can be optimized to ~1–2 nm by using a thinner channel and a thinner gate dielectric layer[45].

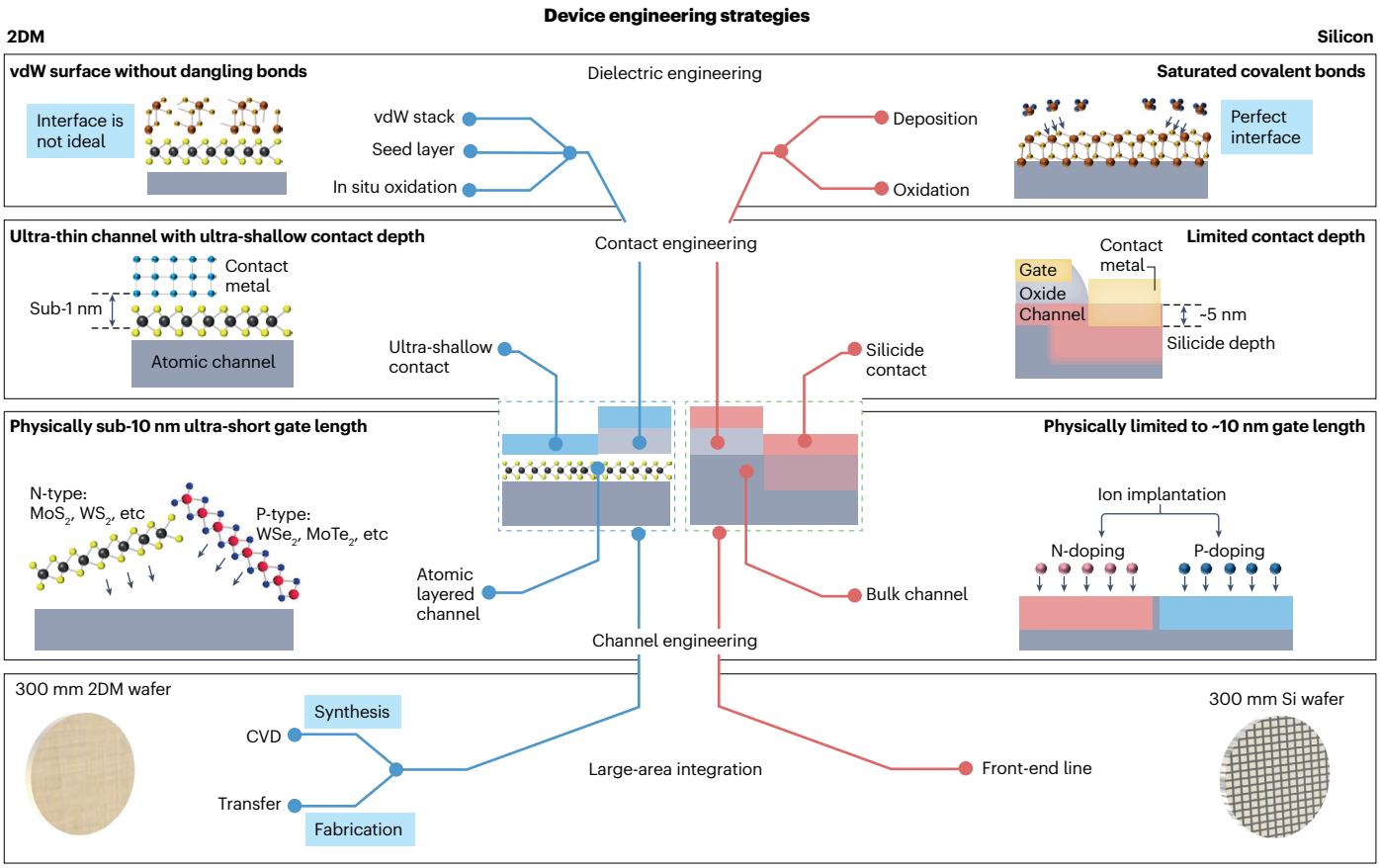
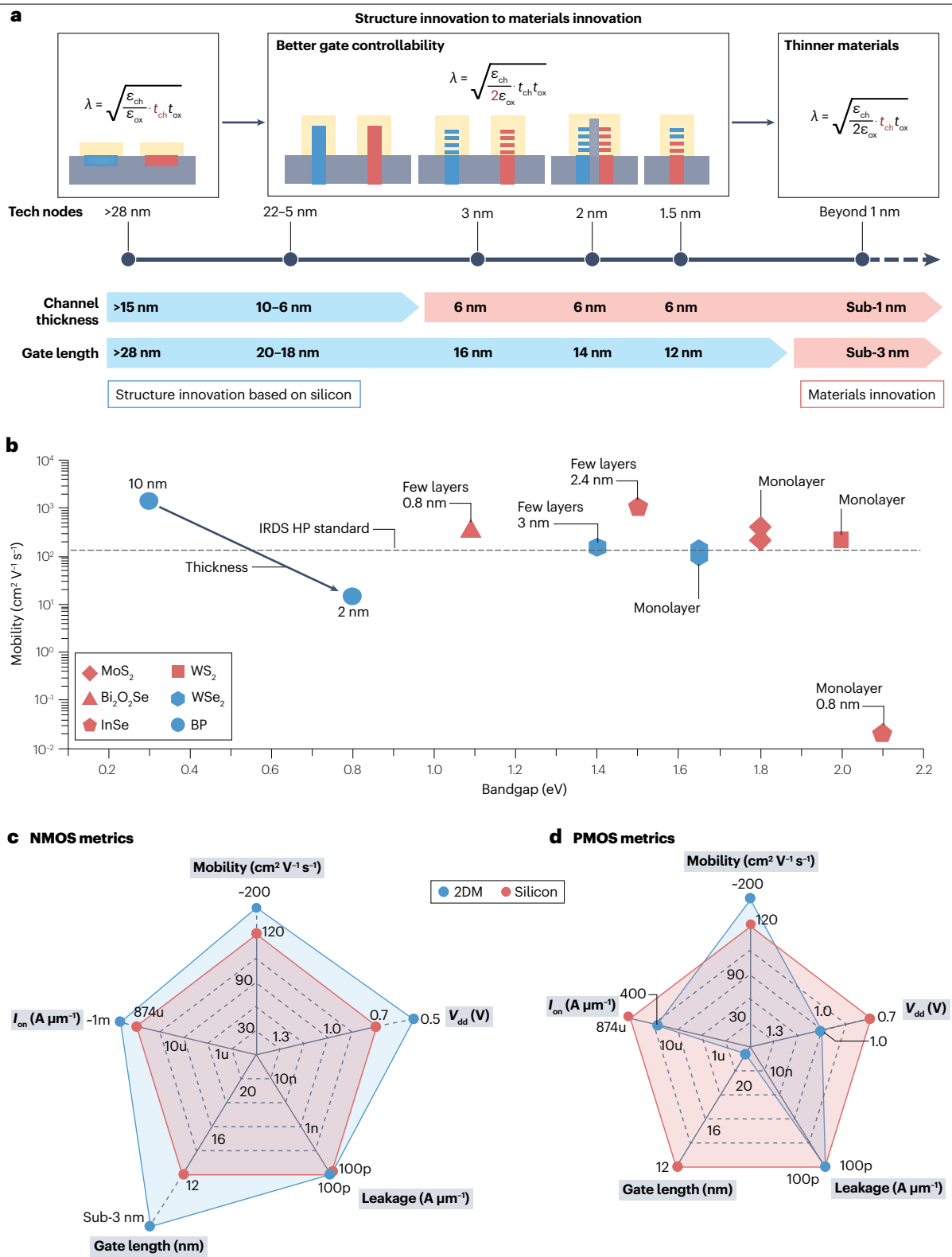


Fig. 1 | Device engineering strategies for 2DMs and silicon technologies. Engineering of dielectric, contact, channel and integration in the 2D materials (2DMs) trend (left). Engineering of dielectric, contact, channel and integration in the silicon trend (right). CVD, chemical vapour deposition; vdW, van der Waals.

The device mobility versus materials bandgap (Fig. 2b) provides an important metric when comparing the most promising 2DMs with silicon. MoS_2 is the most studied 2D n-type semiconductor with a theoretically predicted electron mobility of 410 $cm^2 V^{-1} s^{-1}$ for a monolayer[46]. Provided that defects are inevitably introduced in the device fabrication process, the field-effect mobility is often degraded. Even so, the experimentally verified MoS_2 electron mobility exceeds 200 $cm^2 V^{-1} s^{-1}$ at room temperature, which meets the IRDS requirements for sub-3 nm nodes[22]. Two-dimensional InSe has experimentally demonstrated to exhibit ultra-high electron mobility exceeding 1,000 $cm^2 V^{-1} s^{-1}$ for a few-layer InSe (three layers ~2.4 nm), but it drops sharply to 0.02 $cm^2 V^{-1} s^{-1}$ in a monolayer[32,47]. The mobility degradation may be related to moisture and oxygen in the environment[47], and more experiments are needed to improve the performance of monolayer InSe FET. Another promising 2D semiconductor, Bi_2O_2Se, has a bandgap and electron mobility similar to silicon, and differs from silicon in that its performance metric is not degraded even at a monolayer thickness of 0.61 nm (ref. 48). In addition, the native oxide Bi_2SeO_5 can serve as a gate dielectric for Bi_2O_2Se, which provides a promising route for further scaling[33,48,49].

As a 2D p-type semiconductor, monolayer WSe_2 shows a hole mobility of more than 140 $cm^2 V^{-1} s^{-1}$, satisfying the IRDS requirement for the nodes beyond 3 nm (refs. 47,50–52). P-type boron phosphide has attracted attention owing to its high mobility, but the mobility degrades severely at the thickness below 3 nm (ref. 53). The synthesis of high-quality, few-layer boron phosphide films on the centimetre scale was demonstrated by the controlled pulsed laser deposition strategy[54]. However, for the practical application, more research is needed to solve its instability in the atmosphere[55,56]. Overall, 2DMs show promising results for ultimate scaling with both n-type and p-type materials, demonstrating good mobility at a channel thickness below 3 nm. Figure 2c,d compares the performance metrics of 2DM and silicon transistors, including the on-state current, off-state leakage current, mobility, gate length and operating voltage. It is worth noting that for n-type devices, the performance of 2DMs fully complies with the IRDS standard requirements. Moreover, because the gate length can reach the limit of 1 nm (refs. 57–59), n-type devices have the potential to be applied in sub-1 nm nodes. However, the superior performance of N-channel metal–oxide–semiconductor (NMOS) cannot compensate for the performance shortcomings of 2D P-channel metal–oxide–semiconductor (PMOS) devices. Despite its high mobility, monolayer WSe_2, the on-state current does not match NMOS devices owing to the lack of appropriate metal contact engineering. Although basic CMOS functions can be achieved on a small scale by means of electrostatic regulation, contact metal work function regulation and selective growth channels, the performance of PMOS under the ultimate size is not ideal at present[60–63]. As a result, 2D CMOS devices with superior



performance for advanced tech nodes are yet to be demonstrated. We believe that the development of PMOS should receive more attention in the future study of 2D channel engineering.

Contact engineering for ultra-thin channel

With further device miniaturization, the size of the gate, source and drain active regions of a transistor will become smaller, whereas their

Fig. 2 | Channel engineering of the 2DM transistors. a, Silicon-based transistor scale paths. Device scaling is shifting from structural innovation to material innovation. The mismatch among channel thickness, gate length and tech node becomes more and more intense from the ~22 nm node. Since 3 nm node, channel thickness limits the scaling of the physical gate length. **b**, The relationship between mobility and bandgap in different 2D materials (2DMs)[22,27,46,47,49,52–54,136–140]. **c**, The radar chart comparison of N-channel metal–oxide–semiconductor (NMOS) performance between the 2DM trend and the silicon trend. The parameters represented by each edge are mobility, V_{dd}, leakage, gate length and I_{on}. The biggest advantage of 2DM lies in its ultimate physical gate length. **d**, The radar chart comparison of P-channel metal–oxide–semiconductor (PMOS) performance between the 2DM trend and the silicon trend. IRDS, International Roadmap for Devices and Systems.

equivalent series resistance is expected to increase, adversely affecting the performance of the transistor[64]. To reduce the contact resistance, a technique has been developed in which a metal layer is deposited on the contact area, followed by a subsequent heat treatment to form a silicide, a metal silicon alloy[65,66]. Silicides show stable properties even upon high-temperature heat treatment after alloying, which can significantly reduce defects at the metal–silicon interface, lower the Schottky barrier and drive dopant atoms towards the interface[67].

Increasing the depth of the silicide results in the reduced doping concentration at the interface between silicide and silicon, which in turn leads to a higher contact resistance. Therefore, in the manufacturing process, the depth of the silicide should not exceed half the depth of the junction. Because of the continuous scaling, both the junction depth and contact length decrease with the gate length (Fig. 3a). To maintain the drive current for optimal device operation, the doping in the source–drain area should be used to reduce the contact resistance, which means that a higher doping concentration within shallower junction depths is needed. Thus, continued reliance on the conventional source–drain structure will inevitably challenge the manufacturing process in its capability of producing doped contact regions.

In a 2DMs FET, the contact between the metal and the 2D semiconductor is different from that of a silicon FET, and the depth of the 2DM contact region is ultra-shallow (<1 nm). To achieve a high performance 2DM transistor, contact engineering on ultra-thin 2DMs must be considered[68]. Different from the solution of silicides in bulk Si, the interface between metals and 2DMs in a top-contacted FET configuration can be formed, in most case, only via a van der Waals (vdW) gap. As such, a tunnelling barrier is introduced between the metal and the channel, suppressing charge injection, which manifests in a contact resistance several orders of magnitude higher than the theoretical quantum limit[69]. Therefore, much effort has been dedicated to the issue of contact resistance in 2DMs. In earlier research, metals with low work functions, such as XX, were used to form metal–semiconductor (M–S) junctions with low Schottky barriers to ensure low contact resistance[70]. However, experimentally this approach proved hard to realize, because of the inevitable chemical disorder and Fermi-level pinning at a typical M–S interface. For improved transistor performance, a good metal–channel interface is as important as that between the dielectric and the channel. Standard device fabrication methods often introduce additional defect-induced states, hence the Fermi-level pinning[71]. One effective low-energy and damage-free metal integration strategy entails transferring metals onto 2DMs, which yields a good M–S interface and de-pinning of the Fermi level[72]. However, the contact resistance of 2DMs MOSFETs is still much higher than that of silicon MOSFETs[31].

Several studies have shown that another source of degradation of the contact resistance in 2DMs is metal-induced gap states (MIGSs)[73,74]. MIGSs are formed in the junction owing to the decaying metallic wavefunction with the nanometre penetration depth into the semiconductor. The corresponding solution to this is to use semimetals as M–S contacts. Semimetals are characterized by a density of states near zero at the Fermi level. If the Fermi level of the semimetal is close to the bottom of the semiconductor conduction band, the MIGS contributed by the conduction band can be substantially reduced. Bismuth is a suitable semimetal as a contact metal for MoS_2, showing experimental contact resistance R_c of 123 Ω μm (ref. 34). Similarly, by using semimetal antimony (Sb) $(01\bar{1}2)$, the contact resistance can be further reduced to 42 Ω μm, coming close to the quantum limit for a metal–2DMs contact[75]. Heavy doping of the contact region could result in an ohmic contact, but it is challenging to achieve in an ultra-thin 2DMs channel. Another promising approach relies on ultra-shallow contact doping technology, and the doping depth in ultra-thin 2DMs is below 1 nm (ref. 32). Through theoretical calculations, yttrium (Y) has been found to be the most suitable replacement doping metal in 2D InSe. The yttrium-doping-induced phase transition could lead to an ohmic contact InSe MOSFET and the contact resistance as low as 62 Ω μm.

In the context of scaling, the contact length decreases along with the gate length[76]. The contact length of silicon-based transistors has reached ~10 nm at the latest tech node[31]. In transistor devices, contact resistance is closely related to the contact area or contact length. In the weak-coupling limit, the contact resistance can be estimated by[77–79]

$$R_c = \sqrt{\rho^{2D} r_c}\coth\left(L_{cont}\sqrt{\frac{\rho^{2D}}{r_c}}\right)$$

in which ρ^{2D} is the semiconductor sheet resistivity, r_c is the M–S interface resistivity and L_{cont} is the contact length. Owing to the current crowding, the contact resistance does not depend linearly on the contact length. When the contact length is much larger than the transmission length $\sqrt{\frac{r_c}{\rho^{2D}}}$, the contact resistance is constant and independent of the length. Therefore, to determine conclusively whether the new metal contact strategy is suitable for transistors of ultimate size, it is instrumental to study and fabricate contacts with ultra-short lengths. However, the scaling behaviour of metal–2D semiconductor contacts has been largely neglected. Most studies in contacting 2DMs report L_{cont} dimensions from hundreds of nanometres to a few micrometres. These advanced 2D contact works are a good demonstration of possible future contact engineering and solution strategies for 2DMs. Although excellent performance of contact resistance has been achieved (Fig. 3b), there is still room for improvement in the ultimate scaling of the contact length. In particular, edge contact could provide a path towards ultra-short contact length scaling[80,81]. Density functional theory calculations show that the edge contact leads to a shorter bonding distance with stronger hybridization. However, because the thickness of the 2DMs is limited to one to several atomic layers, it is technically problematic to form pure edge contacts in a large-scale circuit with the existing lithography techniques. For example, 2D edge contact and a low R_c of 670 Ω μm have been achieved on monolayer WS_2 (ref. 82). Owing to its ultra-short contact length, this approach

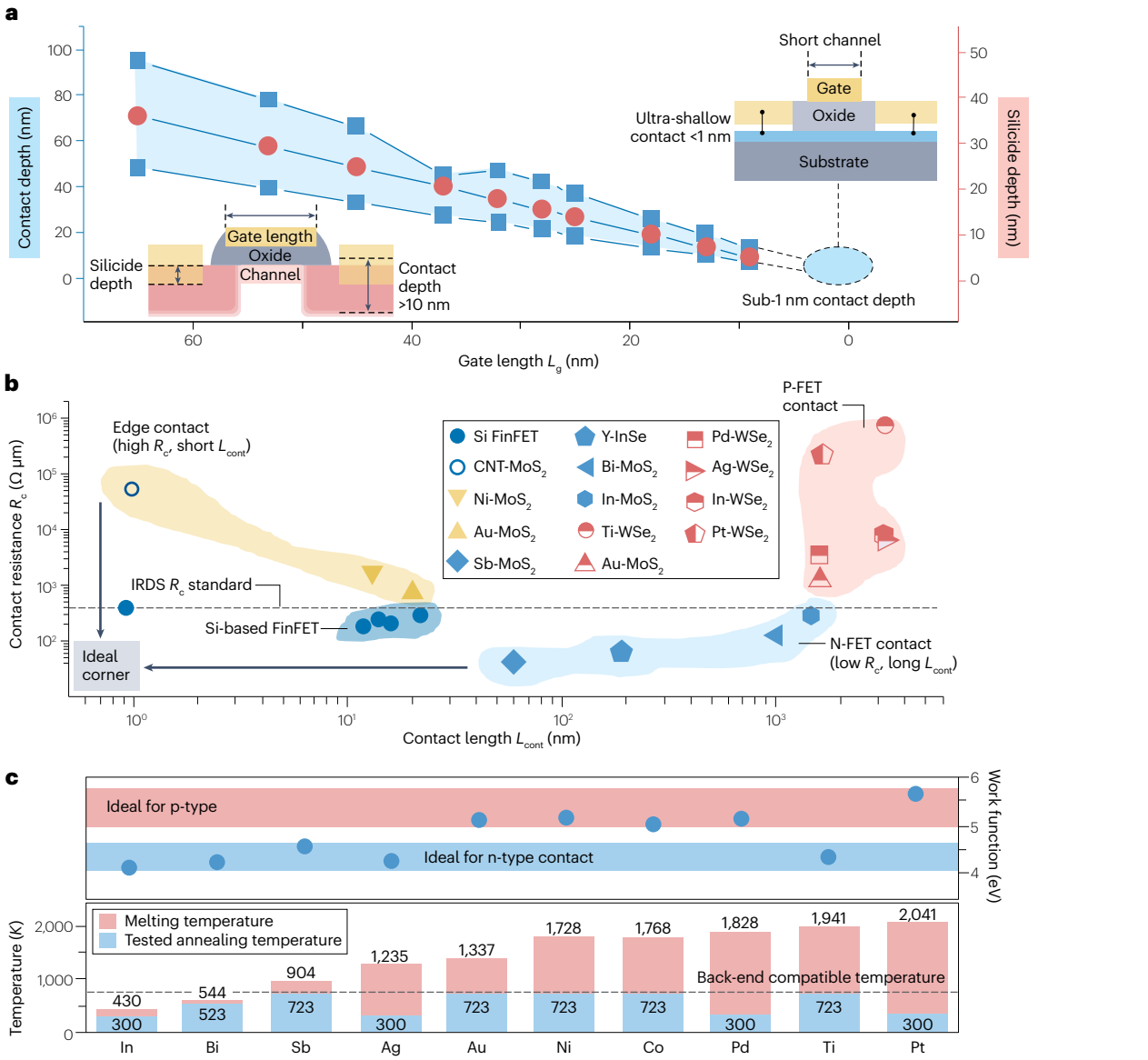


Fig. 3 | Contact engineering of the 2D materials transistors. a, Diagram of the relationship between the junction depth of the active region and the gate length under the silicon-based technology route. The red area represents the depth range of the junction, and the blue ball represents the depth of the silicide layer[6,141]. **b**, Two-dimensional materials contact resistance versus their contact length[24,31,32,34,75,85,87,142–147]. The pink areas represent P-channel field-effect transistor (P-FET) contact. The blue areas represent N-channel field-effect transistor (N-FET) contact. The green areas represent edge contact. The black ball represents the contact in advanced fin field-effect transistor (FinFET). **c**, Diagram of metal work functions. The metal in the red area is suitable for P-type contacts, and the metal in the blue area is suitable for N-type contacts (top). The melting temperature of the metals and the tested annealing process temperature of the transistor with the corresponding metal contact (bottom). CNT, carbon nanotube; IRDS, International Roadmap for Devices and Systems.

provides a possibility for the applications of 2DMs devices with ultra-short contact length.

Recently, metallic single-walled carbon nanotubes (SWCNTs) have been demonstrated to be a good contact material choice for 2DMs[83,84]. Owing to the perfect quasi-1D single-crystal structure, long-distance ballistic transport behaviour and high-current-carrying capacity, SWCNTs can serve as a contact with a sub-1 nm contact length. Using SWCNTs as a contact in MoS_2 FETs results in the realization of the tunable Schottky barrier height[85]. According to the theoretical calculations, the resistance of the CNT contact can be reduced to 419 Ω μm at the ultimate contact length of 1 nm, which can be further optimized by improving the interface quality.

These approaches in advanced 2DM contact engineering have independently demonstrated their scaling potential at ultra-low contact resistance and ultra-short contact length for optimum performance (Fig. 3b). However, it is worth noting that the reported examples

are mainly based on NMOS. To build high-performance CMOS, PMOS with compatible performance is essential. However, the research on high-performance PMOS is lacking. Although there are fewer suitable p-type 2DMs than n-type ones, the developed contact engineering can theoretically be extended to p-type materials. Apart from scaling, the contact of 2D PMOS requires metals with high work function[86]. The fundamental challenge in achieving ultra-clean p-type vdW contacts by standard electron beam evaporation on single-layer TMDs is high energy for sublimation required by high work function metals. The deposition of metal atoms onto 2D TMD layers leads to the formation of defects. For example, the formation of p-type FETs with low contact resistances of 3,300 Ω μm and 1,250 Ω μm has been obtained utilizing high work function metal and Se sacrifice layer[52,87].

Finally, with the back-end-of-line thermal budget of ~400 °C in mind, the metal used for contact must have a high melting point and thermal stability because of the temperature. Some commonly used contact metals are listed in Fig. 3c, classified according to their work function and suitability for NMOS and PMOS. However, none of the existing demonstrations of ultra-low contact resistance, such as the semimetal contact (Bi, Sb ($01\bar{1}2$)), ultra-shallow Y-doping contact, contains the verification of the device performance above the back-end-of-line temperature. Therefore, the emphasis of the 2DMs contact research should be both on contact resistance and on thermal stability.

Dielectric engineering for 2DM–insulator interface

The insulating dielectric layer, bridging the gate and the channel, is implemented to prevent leakage and transmit the gate electric field. Surface conductive channel between the source and drain electrodes is generated under the control of this electric field. The physical properties of the channel material, such as conductivity, carrier mobility and impurity concentration, have a direct impact on the current transfer efficiency and the switching speed of the MOSFET. Additionally, the quality of the dielectric and the interface affects the controllability of the gate to the channel, which in turn affects key parameters such as the threshold voltage of the MOSFET, subthreshold slope and leakage current. Therefore, the performance of a MOSFET depends not only on the characteristics of the channel material but also on the quality of the gate insulator interface and the overall performance of the gate insulator.

In particular, the excellent interface of Si–SiO_2 is one of the main reasons why silicon has become the material of choice in the semiconductor technology (Fig. 4a). The number of silicon dangling bonds at the interface can be reduced to the levels below 10^{10} cm^{-2} via gas passivation[88,89]. Apart from Si–SiO_2, there has been a glaring lack of suitable insulating materials, which limits other channel materials from entering the mass market. Similarly, finding a suitable insulator for 2DMs is a big challenge because of their inert surface that provides no nucleation sites. For this reason, the standard oxides deposition techniques cannot be used for 2DMs channels owing to the formation of multiple defects at the 2DM–oxide interface[90,91] (Fig. 4b). Growing oxide films directly by atomic layered deposition (ALD) results in uneven structures that cannot completely cover the surface, which leads to at least two kinds of defects: the interface and dielectric defects. Although these defects can be reduced by various annealing steps, their density is still much higher than that at the ideal Si–SiO_2 interface. To fully exploit the advantages of 2DMs, it is crucial to develop effective strategies to improve the quality of the 2DMs–insulator interface (Fig. 4c). One strategy is to construct a fully 2D vdW-stacked gate dielectric (Fig. 4c, left). As the layers of different 2DMs are connected by vdW forces, the interface traps and defects between the channel and the insulator can be greatly reduced, thus achieving good dielectric extension[92]. The second strategy relies on a seeding layer between the 2D channel and the bulk insulator. For example, a seeding layer can be introduced as a medium for the oxide during ALD growth (Fig. 4c, middle). Another approach is via partial oxidation of few layers of 2DMs and their transformation into native oxides, which maintains the vdW heterostructure between the channel and the oxide (Fig. 4c, right). This process can potentially lead to atomically abrupt and defect-free interfaces, as promising as the Si–SiO_2 interface.

Although the aforementioned technical paths can, in principle, achieve good 2D interfaces, the feasibility of different strategies needs proper engineering evaluation. As far as the interface and dielectric defects are concerned, we use two parameters: density of the interface states (D_{it}) and gate leakage current density to evaluate the three aforementioned strategies. The continuous power scaling requires a device to operate at the lowest possible voltage. To this end, subthreshold swing (SS) has to be small to keep the device in the on state in a low voltage range. The SS of the device is directly related to the interface quality between the insulator and the channel, which can be described as[91]:

$$SS = \ln(10)\frac{k_B T}{q}\left(1+\frac{C_{channel}+qD_{it}}{C_{insulator}}\right)$$

in which $C_{channel}$ and $C_{insulator}$ are capacitances of the channel and the insulator of the dielectric, respectively. The smaller the density of the interface states D_{it}, the closer the SS of the device to the ideal value of 60 mV per decade at room temperature. For D_{it} over 10^{10} cm^{-2} eV^{-1}, the SS requirement for power scaling cannot be perfectly met.

Aggressive scaling of the gate insulator increases direct tunnelling and thus results in large leakage currents even at low voltages. In addition to direct tunnelling through the insulator, the Fowler–Nordheim tunnelling through the bent barrier and trap-assisted tunnelling, which becomes dominant at high defect density, are all performance-limiting factors to consider[93].

On the basis of the existing literature, we compare the performance metrics in three different technological paths (Fig. 4d). The seed-layer-inducing strategy provides closely distributed sites for ALD nucleation, the method of constructing a seed layer including oxidized metal layers, organic molecules, plasma treatment and so on. However, all these approaches are not without drawbacks. For example, widely used metal oxidation processes are affected by the inherent roughness of evaporating metal films as well as by the destruction of high-energy metal ions, which leads to a threshold voltage drift[94]. Plasma and ozone surface treatments involve energetic and reactive substances, which can also introduce defects and interface states. Using 3,4,9,10-perylene-tetracarboxylic dianhydride has been proposed as the molecular seeding layers[95]. Ultra-thin equivalent oxide thickness (EOT) and good dielectric performance can be achieved on a single device, but because the intrinsic dielectric constant of 3,4,9,10-perylene-tetracarboxylic dianhydride is not high, there is still room for improvement in achieving thinner EOT. Additionally, owing to these layers being formed by discrete molecules, the large-scale homogeneous film integration may be challenging. More recently, a kind of inorganic molecular crystal Sb_2O_3 has been tested as the compatible oxide seeding layer between 2D MoS_2 and high-κ HfO_2 (ref. 42). By means of thermal evaporation, an ultra-thin (1 nm) Sb_2O_3 buffer layer is uniformly grown on the surface of the 2DMs at a slow speed. Using this strategy, a good semiconductor-to-insulator

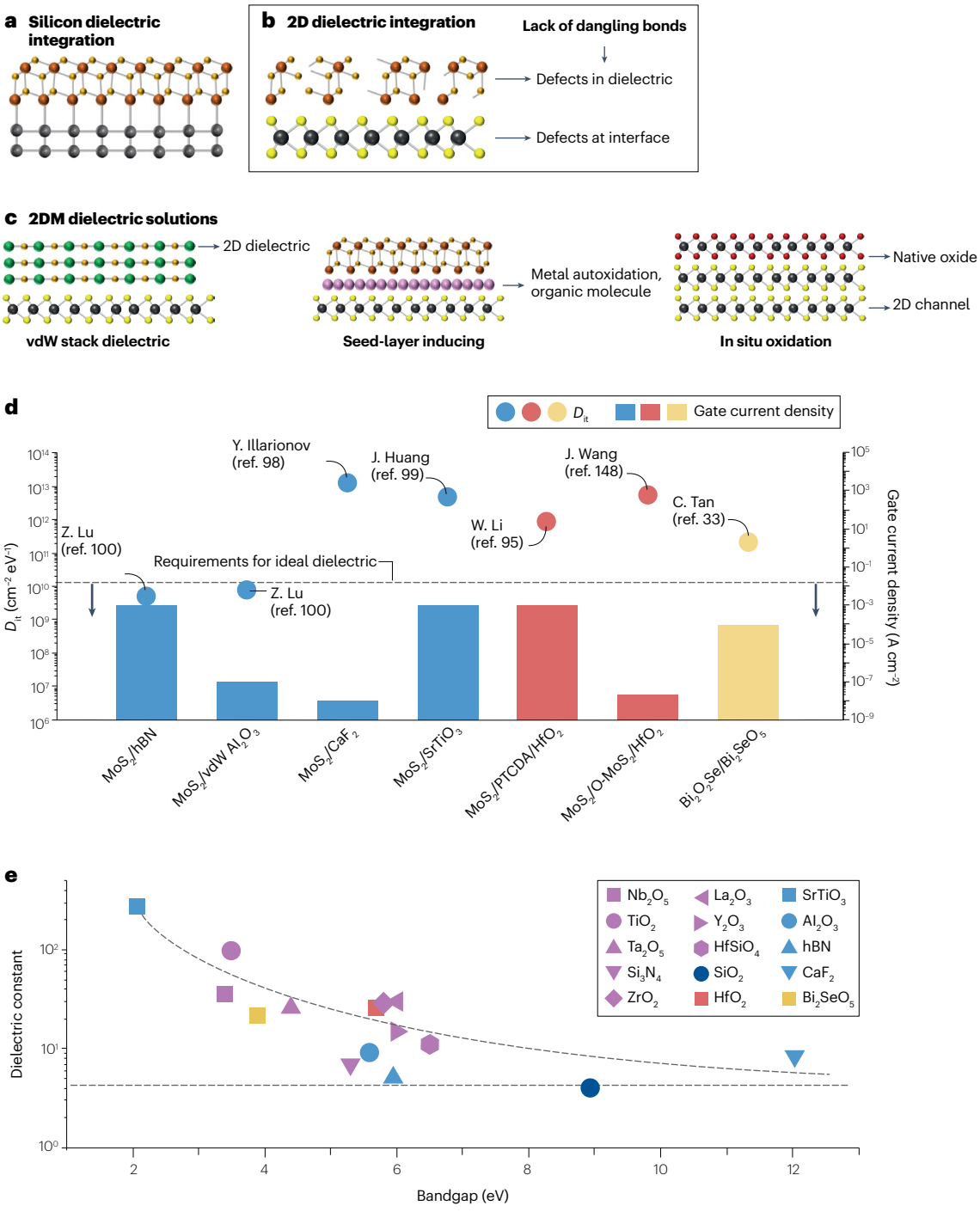


Fig. 4 | Dielectric engineering of the 2DMs transistors. a, Typical bulk silicon oxide dielectric integration. The silicon and the oxide are connected by covalent bonds. **b**, The two kinds of defects when the conventional atomic layered deposition method is used to directly grow the insulation layer on the surface of 2D materials (2DMs): the interface defects and the dielectric defects. **c**, Schematic diagram of the effective strategies for the integration of dielectrics on 2DMs, including van der Waals (vdW) stack dielectric, seed-layer inducing strategy and in situ oxidation. **d**, The quality of the dielectric under several different strategies is summarized, the ball represents the density of the interface state and the column represents the gate leakage current[33,95,96,98–100,148]. **e**, Diagram of the relationship between dielectric constant and bandgap value of different dielectrics. The black colour block represents the traditional bulk material oxide dielectric, and the colourful blocks are the dielectrics that have verified the integration with 2DMs[149,150]. hBN, hexagonal boron nitride; PTCDA, 3,4,9,10-perylene-tetracarboxylic dianhydride.

interface can be formed providing a hydrophilic surface for the deposition of the high-κ dielectric. This type of a seed layer is a promising candidate for the combination of 2DMs and high-κ dielectric. However, it needs to be experimentally verified in small-footprints devices and large-scale circuits. Another strategy of in situ oxidation, which is the partial oxidation of specific 2DMs with the same heterostructure, is also a promising solution for high-quality 2D dielectric engineering for large-scale integration. A relatively new material Bi_2O_2Se with its Bi_2SeO_5 native oxide is one representative system. The most notable point apart from the superior quality of the dielectric Bi_2SeO_5 has a high κ constant (~21), which makes it ideal for the scaling of transistors with small equivalent oxide layer thickness[33,49].

All the aforementioned strategies increase the chances of dielectric integration, but D_{it} remains much higher than that of the Si–SiO_2 interface. Therefore, as the molecular structure of 2DMs is intrinsically different from silicon, we believe that the most potent dielectric engineering strategy is via vdW bonding. Applying 2D crystalline insulators such as hexagonal boron nitride (hBN) to stack vdW dielectric is a promising solution for 2D devices. As an inert and dangling bond-free 2D insulator, hBN has been used as an excellent encapsulation of 2D devices to improve their mobility. Using post-annealing of an MoS_2 channel sandwiched between hBN gate dielectric layers, excellent switching characteristics have been observed with SS of 63 mV per decade and D_{it} of $5 \times 10^9\,cm^{-2}\,eV^{-1}$, on par with silicon technology standards[96]. However, hBN has low dielectric constant (~6) and its bandgap (~6 eV) in bulk is not ideal, which leads to high leakage current at ultra-thin EOT[97]. Therefore, it is difficult to envisage the use of hBN in advanced technology nodes that require ultra-thin insulator thickness. Thus, the defect-free ionic crystal insulators, such as CaF_2 and $SrTiO_3$, have been considered as an alternative to hBN[98,99]. Compared with hBN, these ionic crystals have a higher dielectric constant for further scaling; however, the density of states is significantly increased at the same time, which results in a decrease of the gate capacitance and an increase in the leakage current. Recently, a dry dielectric integration strategy compatible with large areas of 2D devices has been reported[100]. By using polyvinyl alcohol as a sacrificial layer, ultra-thin Al_2O_3 and HfO_2 of sub-3 nm thickness can be pre-deposited and then mechanically dry-released and dry-laminated onto wafer-scale monolayer MoS_2. The 2DMs–insulator interface achieved in this way is different from that obtained by the ALD method. In particular, owing to a weakly coupled vdW dielectric interface, D_{it} is reduced to $7.6 \times 10^9\,cm^{-2}\,eV^{-1}$, which is comparable with the Si–SiO_2 interface. As the dry-transfer process of the dielectric is universal, more bulk materials of high-κ oxide dielectric are expected to be integrated into 2D devices. However, the dielectric layer integration in this strategy is achieved by transfer, which is challenging for high-density integration. The oxide insulators suitable for using as dielectric layer are listed in Fig. 4e. In general, to obtain thinner EOT and smaller leakage, it is necessary to consider a tradeoff between the κ constant and bandgap. As a general rule, most good oxide dielectric materials have a bandgap between 4 eV and 8 eV.

Overall, the existing examples of 2DMs dielectric engineering have proved potent in forming high-quality interfaces, but more systematic optimization schemes are required to explore the validity of these strategies for large-scale transistor circuits. Among the proposed approaches, the use of vdW stack dielectric enables the best interface, but, once again, achieving high-density device integration presents a serious challenge. To this end, seed-layer inducing and in situ oxidation methods have potential to support high-density device integration, but the interface quality has to be improved.

The challenges of bringing 2DMs transistor devices to large-scale integration

Table 1 summarizes the benchmarks of different device engineering technologies from the compatibility to large-scale integration. As mentioned earlier, despite the solid performance of n-type 2DMs MOSFETs, the demonstration of high-performance p-type 2DMs MOSFETs is still lacking. Therefore, going from a single device demonstration to large-scale integration is not a straightforward process. The ultra-thin body and inert surface of the 2DMs makes it impossible to directly integrate them into silicon MOSFETs manufacturing technology. Although the semimetal contact technology and the ultra-shallow doping of a contact region strategy have yielded low contact resistance at a long contact length, the demonstration of good thermal stability of these new technologies is still lacking. Another major challenge is the quality of the 2DM–insulator interface, which needs to be improved to support high-density device integration.

To achieve large-scale integration, the entire front-end process for circuits must be taken into consideration. To this end, it is worthwhile

Table 1 | Benchmarking methods in different transistor engineering

	Methods	Mobility	Gate length	Current	Ready to integrate
Channel engineering	NMOS	★★★	★★★	★★★	★★
	PMOS	★★	–	★★	–
Contact engineering	**Methods**	**Contact resistance**	**Contact length**	**Thermal stability**	**Ready to integrate**
	Ultra-shallow doping	★★★	★★	★	★★
	Semimetal	★★★	★★	★	★★
	Edge contact	★	★★★	★★	★
Dielectric engineering	**Methods**	**Density**	**Interface quality**	**Leakage**	**Ready to integrate**
	vdW stack	★	★★★	★★★	★★
	Seed-layer inducing	★★	★★	★★	★★
	In-situ oxidation	★★★	★★	★★	★★

Two-dimensional device integration technologies, including the channel engineering, contact engineering and dielectric engineering. The number of stars represents the potential of each technical path on the corresponding parameter index. NMOS, N-channel metal–oxide–semiconductor; PMOS, P-channel metal–oxide–semiconductor; vdW, van der Waals.

to compare the fabrication process of silicon-based and 2DMs-based large-scale circuits (Fig. 5).

Self-aligned gates are used to fabricate transistors in silicon-based semiconductor processes and are still used in most modern integrated circuits[101,102]. In the silicon front-end process flow, the relative positions of the gate and source–drain electrodes are defined by the self-aligned process (Fig. 5a). The gate dielectric layer is formed at the beginning of the process and the patterned gate is then deposited on it. The source–drain region is then doped; in the case of polysilicon gate, the gate is doped at the same time. After the doping of the source–drain region, the edge of the doping region defines the channel. The defined channel is always placed perfectly under the control gate, which greatly reduces the parasitic capacitance.

In the 2DMs-based front-end process flow (Fig. 5b), the source and drain electrode regions are defined first, then the dielectric oxide is grown or transferred onto the 2DM channel and electrodes. Finally, a gate electrode is formed on the oxide layer. In this process, to ensure the ability of the gate to control the entire channel, a considerable overlap region is formed between the gate region and the source–drain region. This results in a large parasitic capacitance between the gate and source–drain regions and increases the gate leakage current. According to the Miller effect, the greater the parasitic capacitance C_{gd}, the lower the switching speed[103,104]. Although some researchers have studied the self-aligned process of 2DMs, the performance of oxides integrated in this way needs to be further improved to meet the requirements of IRDS for sub-3 nm nodes[105,106].

Different from the silicon-integrated process, the synthesized 2DMs films are usually transferred to a target substrate. Therefore, the stable synthesis and transfer of wafer-level 2DMs film should also be considered for commercialization of 2DM technology[43,47,54,99,107–125] (Fig. 6a).

Chemical vapour deposition (CVD) is a powerful approach to synthesize 2DMs films on a range of substrates that has been used to grow large-area 2DMs films with controllable thicknesses. Graphene, MoS_2, $MoSe_2$, WS_2, WSe_2, Bi_2O_2Se and hBN films have been successfully grown through well-designed CVD systems at wafer scale[99,112,126–131]. At present, CVD technique enables the growth of single-crystal monolayer films as opposed to earlier demonstration of polycrystalline 2DMs. Recently, the highest room temperature mobility of 232.7 $cm^2 V^{-1} s^{-1}$ in a 4-inch CVD MoS_2 has been reported, showing the feasibility of large-area films with high mobility[123]. An improved CVD synthesis method has been reported that involves a controlled release of precursors and substrates pre-deposited with amorphous Al_2O_3 to ensure uniform synthesis of monolayer MoS_2 as large as 12 inch, suitable for commercialization[124]. The semiconductor industry has been exploring the compatibility of 2DMs with back-end-of-line processes, which practically limits the growth temperature of 2D flakes to that below 450 °C. ALD is a versatile tool suitable for low temperatures. Moreover, because the growth can be controlled at an atomic layer thickness, and the reaction is self-limited to the surface of the substrate, it is, theoretically at least, suitable for the synthesis of 2DMs[132]. At present, only a handful of 2D flakes synthesized by direct growth can meet the IRDS requirements for channel mobility (Fig. 6b).

In small-scale laboratory settings, high-quality 2DM films are still obtained via mechanical exfoliation, which yields random thicknesses and small flake size. Hence, there has been significant motivation to adapt the conventional mechanical exfoliation method to a larger scale. One alternative approach has been to introduce a metal

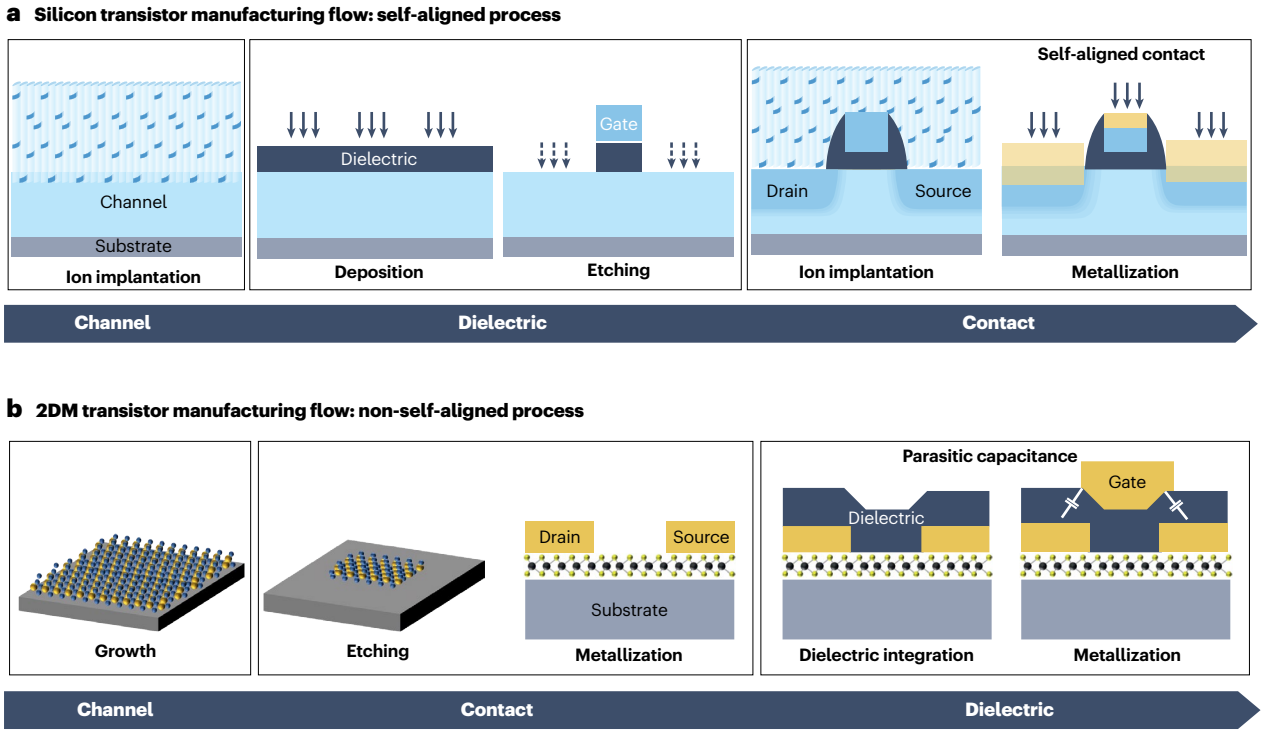


Fig. 5 | Transistor manufacturing flow of silicon and 2DMs. a, Schematic diagram of the typical silicon-based device integration process. The channel is doped by ion implantation, then the gate is defined by atomic layered deposition and polycrystalline silicon mask etching and, finally, self-aligned contact area doping and metallization are achieved. **b**, Schematic diagram of the 2D material (2DM)-based device integration process. Large-scale 2DM channel material growth, the channel is then defined by etching and metallization, the gate dielectric is grown and, finally, the gate electrode is deposited.

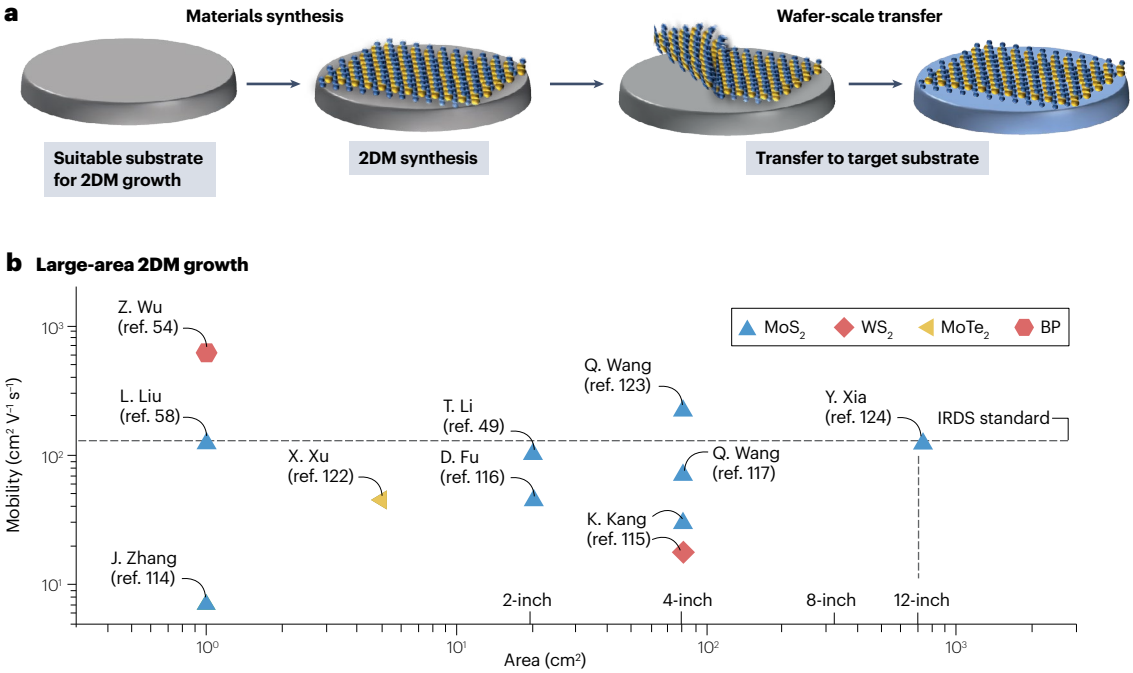


Fig. 6 | Summary of large-area growth of 2DMs. a, Schematic diagram of wafer-level synthesis and transfer of 2D materials (2DMs). **b**, Statistics of mobility and the corresponding area of 2DMs obtained by the synthesis[49,54,58,114,116,117,123,124]. BP, boron phosphide; IRDS, International Roadmap for Devices and Systems.

(for example, Au) or polymeric intermediate substrate to improve the exfoliation yield and lateral size of 2D flakes[133]. With this method, a few millimetre uniform and high-quality 2D flakes can be obtained, which could be used in small-scale circuit function verification. The liquid-phase exfoliation is another well-established laboratory-scale method to obtain 2DMs. However, these methods are not fit for large-scale integrated circuits.

Transferring 2D films onto desired substrates is a key step for the integration of 2DM. Depending on whether chemical solvents are used in the transfer process, they can be broadly divided into two categories: dry transfer and wet transfer. For dry transfer, the usual process involves stripping of a 2DM from its substrate onto an organics stamp (usually polydimethylsiloxane) and then, with the use of a microscope, affixing the stamp with the adhered 2DM to a target substrate. Finally, a heat treatment is used to remove the stamp from the substrate, thus completing the transfer. Dry transfer technique is suitable for most 2DMs and avoids the introduction of unwanted contaminants as the process does not rely on chemical solvents. However, limited by the adhesion between the organic stamps and the 2DMs, the sample size of the transferred flakes does not exceed several centimetres. To this end, a modified dry transfer method has been proposed[100]. The method proceeds through the following steps: first, an organic sacrificial layer is covered on the original substrate, then insulator is pre-deposited on the sacrificial layer and finally the insulator is mechanically dry-released from the original substrate and laminated on the top of wafer-scale MoS_2 through the sacrificial layer. Through this approach, 2-inch 2DM-compatible dry dielectric transfer can be achieved, enabling 2DM dielectric integration.

Wet transfer is usually used in conjunction with CVD technology. 2DMs obtained via CVD are typically grown on metal substrates or foils; therefore, they tend to adhere more strongly to the original substrate, a peel-off step hard to perform. Wet transfer involves spin-coating of an organic layer onto 2DM grown on a metal substrate. Then, the substrate is etched with a chemical solution and dried to obtain an organic support layer in contact with the 2DMs film. Finally, the 2DM film is transferred onto the target substrate following the same method as dry transfer. Compared with dry transfer, wet transfer is more suitable for large-area film transfer of 2DMs because the strength of adhesion of the substrate to the 2DMs is not a consideration. However, because

Table 2 | Benchmarking methods in materials synthesis and wafer-scale transfer

	Methods	Scale	Quality	Integration compatibility
Materials synthesis	Chemical vapour deposition	★★★	★★★	★★★
	Atomic layered deposition	★★	★★	★★
	Mechanical exfoliated	★	★★★	★
	Solution exfoliated	★★	★★	★
	Methods	**Scale**	**Yield**	**Integration compatibility**
Wafer-scale transfer	Dry transfer	★★	★★	★★★
	Wet transfer	★★	★★	★★
	Wafer bonding	★★★	★★	★★
	Metal assistant	★	★	★

A summary table of different material synthesis methods and wafer-level transfer processes. The number of stars represents the potential of each technical path on the corresponding parameter index.

chemical solvents are introduced in the transfer process, it is likely to lead to film breaking, wrinkling and bending. Owing to the different wettability of 2DM films and the growth substrates, 2DM films can be easily and quickly delaminated by deionized water at room temperature. As a result, an improved wet transfer method has been reported showing good transfer at a 6-inch size[134]. Drawing on the principle of wet transfer, a metal-assisted transfer approach has also been recently proposed, which is well suited for basic device performance verification in the laboratory owing to the ability to consistently obtain high-quality monolayer 2DMs[133]. In particular, wet transfer technology has been proposed based on wafer-bonding machines for large-scale semiconductor manufacturing lines[135]. The study claims to have successfully transferred monolayer WS_2 and some other 2DMs between 300 mm wafers by utilizing bisbenzocyclobutene as an adhesive sacrificial layer, which could prove promising if extended to other 2DMs. In principle, both dry and wet transfer methods can be used for wafer-scale 2DM transfer. More commercial equipment and technical methods need to be developed to improve transfer efficiency. Finally, the material synthesis and transfer techniques are summarized in Table 2. To accelerate the 'lab-to-fab' transition of 2DMs, work on large-scale growth and wafer-scale transfer processes should be intensified.

Outlook

Owing to high performance at atomic thicknesses, 2DMs open up the possibility of further transistor miniaturization beyond the limits of bulk materials. Building upon the extensive experience of the continued innovation in silicon MOSFET technology and through the optimization and further development of channel, contact and dielectric engineering approaches, 2DMs could deliver a breakthrough in the device performance at the ultimate scale. For that, the optimization of 2D transistors has to be approached holistically, by considering different types of device engineering. As far as the overall front-end process is concerned, the self-aligned integration process, high-quality wafer-scale 2DMs synthesis and transfer should be completed.

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Author contributions

P.Z. and C.L. provided innovative ideas for the article, and S.Z. and C.L. worked together on the organization and writing of the article. The authors reviewed the novel solutions for channel, contact and dielectric engineering using 2DM to address the scaling challenges at the advanced tech node. Channel engineering for 2DM transistors is reviewed. The authors suppose that further research should be conducted on the PMOS channel. The contact engineering of 2DM transistors is reviewed, and the contact technology of 2DM is summarized in terms of contact resistance, contact length and process temperature compatibility. The authors summarized the three promising dielectrics engineering of 2DM transistors and analysed the advantages and disadvantages of each path. The fabrication processes of 2DM and silicon transistors are compared in this Review, and the importance of self-aligned manufacturing process of 2DM transistors is emphasized. The authors summarized the challenges in translating the performance of individual 2DMs devices into large-scale integration, including large-scale 2DM transfer, as well as controllable high-quality synthesis of 2DM.

Competing interest

The authors declare no competing interests.

Additional information

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